d) Remarks

d.1. Specification

The title of the invention stands objected to as being not descriptive. The Applicants have accordingly provided a new title, as indicated above.

d.2 Claim Rejections - 35 U.S.C. §103

Claims 1-4, 9-11, 3-16, and 20-22 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent no. 4,682,284 (hereinafter referred to as Schrofer) in view of U.S. Patent no. 5,954,815 (hereinafter referred to as Joshi).

The Applicants have, responsive to this rejection, amended the independent claims of the present application to include limitations from canceled dependent claims. Specifically, claim 1 has been amended to include the limitations of canceled claim 3, claims 13 has been amended to include the limitations of canceled claim 15, and claim 21 has been amended to include limitations corresponding substantially to those of canceled claim 3.

To establish a **prima facie** case of **obviousness**, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claim 1, as amended, includes the following limitation:

"In a queue, writing a first instruction of a plurality of instructions to a first location indicated by a write pointer, the plurality of instructions being written to the queue as a set of a predetermined number of instructions, and the first instruction of the plurality of instructions being indicated as invalid on account of being outside a trace of instructions;" (Emphasis Added).

In rejecting canceled claims 3 and 15, the Office Action contends that the combination of Schrofer and Joshi teaches that a plurality of instructions are written to a queue as a set of a predetermined number of instructions, and wherein at least one instruction of the set is indicated as being invalid by an associate valid bit on account of being outside a trace instructions (paragraph 8 of the Office Action).

The Applicants respectfully disagree. Joshi, in pertinent part, discloses the following:

Apparatus 30 includes an instruction cache 34 which stores a plurality of lines of instructions that may be addressed by an address value received on a communication path 38. In this embodiment, each line stores four 32-bit instructions and communicates all the instructions in a line to a predecode circuit 42 over a communication path 46. Predecode circuit partially decodes the four instructions and communicates the four partially decoded instructions to an instruction queuer 50 over a communication path 54 and to dispatch multiplexers 58A-D over a queue bypass path 62. (Joshi, column 4, lines 1-11). (Emphasis Added).

In general, a new line of instructions is read from instruction cache 34 on every clock cycle. If four instructions were dispatched every clock cycle, then dispatch register would always be loaded from queue bypass path 62. (Joshi, column 4, lines 51-52). (Emphasis Added).

The value in source field 132 is communicated to a valid mask 148 through an OR circuit 150. If the branch is predicted, valid mask 158 invalidates all instructions in the current line which occur after the delay instruction associated with the branch, since they would not be executed if the branch were taken. For example, if the delay instruction is the third instruction in

the line as shown in FIG. 7, then the fourth instruction will be invalidated. During the next clock cycle, the line (including any invalidated instructions) are communicated to instruction queuer 50 and queue bypass path 62 (FIG. 3), the value of the destination field is loaded into a register 152, the value of counter 116 is loaded with the value from index field 128, and instruction cache 34 is addressed to fetch the line which contains the predicted branch target instruction. The destination field in register 152 is then communicated to valid mask 158 through OR circuit 150 to invalidate the instructions which occur before the branch target instruction in the line. For example, if the branch target instruction is the second instruction in the line, then valid mask 158 invalidates the first instruction in the line. The line is then communicated to instruction queuer 50 and queue bypass path 62. (Joshi, column 7, lines 1-21). (Emphasis Added).

From the above, it is apparent that Joshi discloses an instruction cache that stores a plurality of lines of instructions, and that a new line is read from this instruction cache every clock cycle. Joshi further discloses that if a branch is predicted, a valid mask invalidates all instruction in a line after a delay instruction associated with the relevant branch.

In contrast, claim 1 requires a first instruction that is indicated as being invalid on account of being outside a trace of instructions.

The Examiner is referred to the exemplary embodiment of the present invention described on page 25, lines 7 - page 27, line 5, with reference to **Figure 7** and **8**. Specifically, this description provides exemplary ways in which "bubbles" may be introduced into a queue. For example, where the number of microinstructions contained in a specific trace in not a multiple of the size of predetermined sets, a partial set of microinstructions may be written to a uop line of a queue.

Independent claims 13 and 21 have been amended to include limitations corresponding substantially to the above discussed limitation of claim 1, the above

remarks are also applicable to a consideration of the allowability of these independent claims.

A number of the remaining dependent claims of the present application also stand rejected under 35 U.S.C. § 103(a) as being unpatentable over various combinations of references. However, as each dependent claim is deemed to include the limitations of the claims from which it depends, the above amendments and remarks also serve to address these rejections.

In conclusion, the Applicants believe that all objections and rejections raised in the Office Action have been address and withdrawal of these objections and rejections is respectfully requested. Furthermore, the Applicants believe that all claims are now in a condition for allowance, which is earnestly solicited.

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of the present application, the Examiner is invited to contact André Marais at (408) 947-8200.

Respectfully submitted,
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